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PATENT APPLICATION

ATTORNEY DOCKET NO. 200302141-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Brown et al.

Confirmation No.: 7276

Application No.: 10/037,541

Examiner: Trimmings, John P

Filing Date: January 4, 2002

Group Art Unit: 2133

Title: Method and Apparatus for Providing JTAG Functionality in a Remote Server Management Controller

Mail Stop Appeal Brief-Patents
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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **05/09/2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
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( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

Andrew Brown et al.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew Brown et al.	§	Group Art Unit: 2133
Serial No.: 10/037,541	§	Examiner: Trimmings, John P.
Filed: January 4, 2002	§	
For: METHOD AND APPARATUS FOR PROVIDING JTAG FUNCTIONALITY IN A REMOTE SERVER MANAGEMENT CONTROLLER	§	Atty Docket: 200302141-1 Comp:0229/FLE/HOF

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July 12, 2005 — Date

David M. Hoffman

Sir:

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance of the Notice of Appeal mailed on May 9, 2005, and received by the Patent Office on May 13, 2005.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be necessary to advance prosecution of the present application, to Account No. 08-0892, Order No. 200302141-1/FLE (COMP:0229).

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1. **REAL PARTY IN INTEREST**

The real party in interest is Hewlett-Packard Development Company, L.P. (hereafter "HPDC"), a Texas Limited Partnership having its principal place of business in Houston, Texas and the Assignee of the above-referenced application. Accordingly, HPDC, as the Assignee of the above-referenced application, will be directly affected by the Board's decision in the pending appeal.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any other appeals or interferences related to this Appeal.

3. **STATUS OF CLAIMS**

Claims 1-25 are currently pending and under final rejection and, thus, are the subject of this appeal.

4. **STATUS OF AMENDMENTS**

No claims have been amended since the final rejection. As such, there are no outstanding amendments to be considered by the Board.

5. **SUMMARY OF CLAIMED SUBJECT MATTER**

The present application is directed to a method and apparatus for providing Joint Test Action Group ("JTAG") functionality in a remote server management controller. Page 2, lines 6-8. The JTAG standard "sets out a methodology for performing testing on complex integrated circuits and circuit boards" using JTAG compatible integrated circuits that have "test functionality built directly into...[their] internal workings." Page 3, lines 18-20; page 5, lines 3-5. The JTAG architecture can be "envisioned as a large scan chain, in which the

JTAG-compatible chips on a circuit board are all connected in series (like a chain) that is accessible [and testable] through the test connector on the circuit board." Page 5, lines 8-11. In one embodiment, a managed server could be configured to allow programming or updating of "JTAG-compatible devices in the managed server...remotely and without the need for an on-site service call." *See* page 39, lines 2-4.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a remote server management controller (*e.g.*, 200) disposed in a managed server (*e.g.*, 20). *See, e.g.,* page 16, lines 16-20; page 17, lines 12-15; *see also* Figs. 1 and 2. The remote server management controller comprises an IOP (*e.g.,* 302). *See, e.g.,* page 18, lines 15-19. The remote server management controller also comprises an embedded JTAG master (*e.g.,* 404) that is controllable by the IOP, wherein the embedded JTAG master has a JTAG interface (*e.g.,* 406). *See, e.g.,* page 22, lines 14-20. The remote management controller further includes at least one integrated circuit (*e.g.,* 600) disposed in the managed server and connected for operative communication to the JTAG interface. *See, e.g.,* page 24, lines 14-18. The JTAG master (*e.g.*, 404) is configured to be accessed remotely through the remote server management controller to provide communication between a remote computer (*e.g.,* 42 or 72) and the at least one integrated circuit via the JTAG interface. *See, e.g.,* page 16, lines 16-20; *see also*, Fig. 1.

With regard to the aspect of the invention set forth in independent claim 9, discussions of the recited features of claim 9 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present

invention relates to a managed server (*e.g.*, 20). *See, e.g.*, page 16, lines 16-20. The managed server comprises a motherboard having at least one integrated circuit (*e.g.*, 600) disposed thereon. *See, e.g.*, page 24, lines 14-18. The managed server also includes a remote server management controller (*e.g.*, 200) in operable communication with the managed server. *See* page 17, lines 12-15; *see also* Figs. 1 and 2. The remote server management controller comprises an IOP (*e.g.*, 302). *See, e.g.*, page 18, lines 15-19. The remote server management controller also includes an embedded JTAG master (*e.g.*, 404) that is controllable by the IOP, the embedded JTAG master having a JTAG interface (e.g., 406), wherein the at least one integrated circuit is connected for operative communication to the JTAG interface. *See, e.g.*, page 22, lines 14-20, page 24, lines 14-18. The JTAG master is configured to be accessed remotely through the remote server management controller to provide communication between a remote computer (*e.g.*, 42 or 72) and the at least one integrated circuit via the JTAG interface. *See, e.g.*, page 16, lines 16-20; *see also*, Fig. 1.

With regard to the aspect of the invention set forth in independent claim 16, discussions of the recited features of claim 16 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of communicating with an integrated circuit (*e.g.*, 600) in a managed server (*e.g.*, 20), the managed server having a remote server management controller (*e.g.*, 200) in operative communication therewith, the remote server management controller having an IOP (*e.g.*, 302) and a JTAG master (*e.g.*, 404) disposed thereon for operative communication with each other, the JTAG master having a JTAG interface (*e.g.*, 406) connected for operative communication to the integrated circuit. *See, e.g.*, page 16, lines 16-20; page 17, lines 12-15; page 18, lines 15-19; and page 22, lines 14-20, page 24, lines 14-18; *see also*, Figs. 1 and 2. The method comprises the act of receiving

data at the IOP of the remote server management controller. *See, e.g.,* page 20, lines 1-9. The method also includes transmitting the data from the IOP to the JTAG master. *See, e.g.,* page 21, lines 19-21. The method also comprises transmitting the data from the JTAG master to the integrated circuit via the JTAG interface. *See, e.g.,* page 24, lines 14-21.

With regard to the aspect of the invention set forth in independent claim 21, discussions of the recited features of claim 21 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of using a computer (*e.g.,* 42 or 72). *See* page 16, lines 4-9. The method comprises connecting a computer to a remote server management controller (*e.g.,* 200) disposed in a managed server (*e.g.,* 20). *See, e.g.,* page 16, lines 16-20; page 17, lines 12-15; *see also* Figs. 1 and 2. The method also includes communicating with an integrated circuit (*e.g.,* 600) disposed in the managed server via a JTAG interface (*e.g.,* 406) associated with the remote server management controller. *See, e.g.,* page 16, lines 16-20; page 24, lines 14-21.

With regard to the aspect of the invention set forth in independent claim 24, discussions of the recited features of claim 24 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of manufacturing a computer (*e.g.,* 20). *See, e.g.,* page 16, lines 16-20. The method comprises disposing a remote server management controller (*e.g.,* 200) in a server wherein the remote server management controller comprises an IOP (*e.g.,* 302), an embedded JTAG master (*e.g.,* 404) that is controllable by the IOP, the embedded JTAG master having a JTAG interface (*e.g.,* 406), and an integrated circuit (*e.g.,* 600) disposed in the managed server and connected for operative communication to the JTAG

interface. *See, e.g.,* page 16, lines 16-20; page 18, lines 15-19; page 22, lines 14-20, page 24, lines 14-18; and page 24, lines 14-21. The JTAG master (as employed in the method) is also configured to be accessed remotely through the remote server management controller to provide communication between a client computer and the integrated circuit via the JTAG interface. *See, e.g.,* page 16, lines 16-20; page 24, lines 14-21.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants respectfully urge the Board to review and reverse the Examiner's ground of rejection in which the Examiner rejected claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (U.S. Patent No. 6,598,193, hereafter "the Li reference") in view of Falik et al. (U.S. Patent No. 6,065,078, hereafter "the Falik reference").

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting claims 1-25 under 35 U.S.C. § 103(a). Accordingly, Appellants traverse these rejections and respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-25 are currently in condition for allowance.

1. Judicial precedent has clearly established a legal standard for a *prima facie* obviousness rejection.

First, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). To establish a

prima facie case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d. 1430 (Fed. Cir. 1990).

Second, the Examiner must also provide *objective evidence*, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to modify a cited reference. *In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002). A mere statement that the proposed modification would have been "'*well within the ordinary skill of the art*'" based on the Examiner's knowledge of the claimed elements cannot be relied upon to establish a *prima facie* case of obviousness without some *objective reason to combine* the teachings of the references. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (B.P.A.I. 1993); *In re Kotzab*, 217 F.3d 1365, 1371, 55 U.S.P.Q.2d. 1313, 1318 (Fed. Cir. 2000); *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 U.S.P.Q.2d. 1161 (Fed. Cir. 1999). Moreover, an admitted deficiency in a cited reference cannot be remedied by the Examiner's "general conclusions about what is 'basic knowledge' or 'common sense' to one of ordinary skill in the art. *See In re Zurko*, 59 U.S.P.Q.2d 1693, 1697 (Fed. Cir. 2001). Specifically, the Examiner is not permitted to "reach conclusions based on ...[the Examiner's] own understanding or experience — or on...[the Examiner's] assessment of what would be basic knowledge or common sense." *See*

id. Rather, the Examiner must present concrete evidence to establish a *prima facie* case of obviousness.

Third, when prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself; in other words, something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Fourth, if the Examiner relies on a theory of inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *In re Robertson,* 169 F.3d 743, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999). The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. *Id.* In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art. *Ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990). The Examiner, in presenting the inherency argument, bears the evidentiary burden and must adequately satisfy this burden. *See id.*

Fifth, it is only appropriate for an Examiner to take Official Notice of facts not in the record, when those facts are "capable of such instant and unquestionable demonstration as to

defy dispute" *In re Ahlert*, 165 USPQ 418, 420 (C.C.P.A. 1970) *citing In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961). Furthermore, assertions of technical facts in the areas of esoteric technology are not appropriate for Official Notice and must always be supported by citation to some reference work recognized as standard in the pertinent art. *Id.* at 420-21.

2. **The Examiner's rejections of independent claims 1, 9, 21, and 25 are improper because the cited references fail to disclose communication between a remote computer and an integrated circuit via the JTAG interface.**

Appellants respectfully assert that communication between a remote computer and an integrated circuit via a JTAG interface, as recited in independent claims 1, 9, 21, and 24, is not disclosed or suggested by the cited references. For example, independent claims 1, 9, and 24 recite a JTAG master that is "configured to be accessed remotely through the remote server management controller to provide *communication* between a remote computer and the at least one integrated circuit *via the JTAG interface*." (Emphasis added). Independent claim 21 recites "connecting a computer to a remote server management controller" and "communicating with an integrated circuit...*via a JTAG interface*." (Emphasis added).

The Examiner's rejections of independent claims 1, 9, 21, and 24 are insufficient to establish a *prima facie* case of obviousness, because the cited references do not teach or suggest, alone or together, the claim features recited above. The Li reference discloses a system and method for testing component IC chips. Abstract, lines 1-2. The system disclosed in the Li reference can be configured to "test one or more component IC chips using the embedded JTAG test routine [within a management controller 102] during boot up of the system." Abstract, lines 8-12. The results of these tests can be stored in server

management storage 112. Col. 4, lines 61-63. Once stored in server management storage 112, the remote systems 126 may "be allowed selective access to management controller 102... *to access a test result* or a log of previous test results" via a phone line 106, internet 123, Ethernet 120, or I^2C controller 108. Col. 5, lines 10-16 (emphasis added). .

This conventional file transfer, however, in no way involves a JTAG master or a JTAG interface. *See* col. 5, lines 10-16. Contrary to the Examiner's assertions, the mere fact that the transferred file happens to include JTAG-based test results does not make a mere file transfer either communication or communicating "via the JTAG interface," as recited in claims 1, 9, 21, and 24. In other words, transferring a file *created by and stored on* the management controller 102 via Ethernet 120 simply is not the communication between a remote computer and an integrated circuit *via the JTAG interface*. The Falik reference cannot cure the above-described deficiencies in the Li reference because the Falik reference does not even disclose a remote computer, much less communication between the non-existent remote computer and an integrated circuit via the JTAG interface, as recited in claims 1, 9, 21, and 24. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 9, 21, and 24 and the claims that depend therefrom.

3. **The Examiner's rejection of independent claim 16 is improper because the cited references fail to disclose transmitting data from the JTAG master to the integrated circuit via the JTAG interface**

Independent claim 16 recites a method of communicating with an integrated circuit in a managed server comprising "receiving data at the IOP of the remote server management controller; transmitting *the data* from the IOP to the JTAG master; and transmitting the data from the JTAG master to the integrated circuit *via the JTAG interface*." (Emphasis added).

However, as described above in regard to claims 1, 9, 21, and 24, the Li reference merely discloses a one-way, conventional file transfer from the management controller 102 to the remote systems 126. *See* col. 5, lines 7-16. In other words, the transfer of data disclosed in the Li reference is clearly directed out of the management controller 102 rather than directed towards the integrated circuit, as recited in claim 16. *See* Li, col. 5, lines 7-16. As such, the Li reference cannot disclose "receiving data at the IOP," and transmitting that "data from the IOP to the JTAG master" and "from the JTAG master to the integrated circuit," as recited in claim 16.

The Falik reference cannot cure the above-described deficiencies in the Li reference because, as will be described in greater detail below, the Falik reference does not disclose an IOP, much less "transmitting data from the IOP to the JTAG master," as recited in claim 16. For this reason, the Falik reference can clearly not cure the above-described deficiencies in the Li reference. As such, Appellants request that the Board overturn the Examiner's rejection and allow independent claim 16 and the claims that depend therefrom.

4. **The Examiner's rejections of independent claims 1, 9, 16, and 25 are improper because the cited references fail to disclose a remote server management controller comprising an IOP.**

Appellants respectfully assert that the references cited by the Examiner do not disclose or suggest, alone or together, a remote server management controller comprising an IOP, as recited in independent claims 1, 9, 16, and 24. For this additional reason, Appellants respectfully assert that the Examiner has not established a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

In the Final Office Action mailed on February 7, 2005, the Examiner conceded that the Li reference "fails to specifically cite an 'IOP' (IO Processor) which would be the 'management controller comprising: an IOP' as claimed." Page 5, lines 14-16. In an attempt to cure this admitted deficiency in the Li reference, however, the Examiner has proffered only a web of "suggestions" and inherency that is completely unsupported by any objective evidence. Specifically, the Examiner stated that "one of ordinary skill in the art *would know* that the management controller of Li et al. would contain a processor," and that "it *would also be well known* that an I/O controller is *suggested* in Li et al." Final Office Action, page 5, lines 16-19 (emphasis added). From these two assertions, the Examiner concluded that "[t]he combination of the two features...strongly suggested to the examiner that the management controller is an I/O (interface with modem/Ethernet) Processor." *Id.*, page 5 line 19 - page 6, line 1.

For a variety of reasons, however, the Examiner's web of "suggestions" and inherency do not rise to the level of a *prima facie* case of obviousness. First, the Examiner's rejection is based on a "strong suggest[ion] to the examiner," – rather than a suggestion to one of ordinary skill in the art. *Id.*, page 5, line 23. As the Board is well aware, however, an admitted deficiency in a cited reference cannot be cured based on the Examiner's "own understanding or experience — or on...[the Examiner's] assessment of what would be basic knowledge or common sense." *See In re Zurko*, 59 U.S.P.Q.2d 1693, 1697 (Fed. Cir. 2001). In other words, to establish a *prima facie* case of obviousness, the Examiner has to establish that the Li reference would suggest an IOP to one of ordinary skill in the art – not merely state that the Li reference suggests an IOP to the Examiner. *See Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Appellants believe that at least part of the reason for the Examiner's unsupported rejection is that the Examiner appears to believe that the Examiner is one of ordinary skill in the art. *See* Final Office Action, page 2, line 22 – page 3, line 1 (stating "[t]he examiner, being one with ordinary skill"). The Board, however, has made it clear that a person of ordinary skill in the art is a hypothetical person – not an Examiner. *See Ex parte Hiyamizu*, 10 U.S.P.Q.2d 1393, 1394 (B.P.A.I. 1988); *see also* M.P.E.P. 2141.03. As such, the Examiner has clearly not applied the correct legal standard in rejecting independent claims 1,9,16, and 25, and therefore could not have established a *prima facie* case of obviousness. For at least this reason, Appellants respectfully request that the Board overturn the Examiner's rejections and allow independent claims 1, 9, 16, and 24 and the claims that depend therefrom.

Second, Appellants respectfully assert that the Examiner's web of "suggestions" is so far attenuated from the actual disclosure of the Li reference that it amounts to hindsight and, as such, cannot establish a *prima facie* case of obviousness. In particular, the Examiner conceded in the Final Office Action that the Li reference did not even directly suggest an IOP. Rather, the "suggestion" for the IOP was built upon two other "suggested" elements – namely a processor and an I/O controller. *See* Final Office Action, page 5, lines 16-19. In other words, to follow the Examiner's reasoning, one of ordinary skill in the art would have to add two admittedly undisclosed elements to the Li reference and then use those two non-recited elements as the basis to add a third undisclosed element. This "bootstrapping" is so unlikely and so far attenuated from the disclosure of the Li reference, that it is clearly based only on the hindsight gained from the invention itself. For at least this additional reason, Appellants respectfully request

that the Board overturn the Examiner's rejections and allow independent claims 1, 9, 16, and 24 and the claims that depend therefrom.

Third, Appellants also respectfully assert that the claim features dismissed by the Examiner as inherent do not meet the legal standards to be considered inherent. In particular, as described above, the Examiner stated in the Final Office Action that "one of ordinary skill in the art *would know* that the management controller of Li et al. would contain a processor." Page 5, lines 16-19 (emphasis added). With regard to the Examiner's apparent claim of inherency, Appellants respectfully assert that a processor does not *necessarily* flow from the management controller of the Li reference. As such, and because the Examiner has not satisfied the Examiner's evidentiary burden to provide a basis in fact and/or line of technical reasoning to reasonably support the claim of inherency, Appellants assert that the Examiner has not established a *prima facie* case of obviousness based on the claim of inherency. *See Ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990).

Fourth, Appellants also respectfully assert that the claim features for which the Examiner used Official Notice do not meet the legal standards to qualify for Official Notice. In particular, as described above, the Examiner stated in the Final Office Action that "it *would also be well known* that an I/O controller is *suggested* in Li et al." Page 5, lines 16-19 (emphasis added). Appellants note that it is only appropriate for an Examiner to take Official Notice of facts not in the record, when those facts are "capable of such instant and unquestionable demonstration as to defy dispute" *In re Ahlert*, 165 USPQ 418, 420 (C.C.P.A. 1970) *citing In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961). As such, Appellants respectfully assert that the presence or absence of a complex, electronic

component, such as an I/O controller, simply cannot be capable of such instant and unquestionable demonstration as to defy dispute." *See id.* Accordingly, Appellants believe that the Examiner's use of Official Notice to "create" a non-existent I/O controller was improper. Furthermore, to the extent that the Examiner appears to believe that the claim of inherency described above was actually Official Notice[1], Appellants also assert that it is improper for the Examiner to use Official Notice to create a processor. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejections based on Official Notice and allow independent claims 1, 9, 16, and 24 and the claims that depend therefrom.

Fifth, Appellants respectfully assert that the Falik reference cannot cure the admitted deficiencies in the Li reference, because the Falik reference also clearly does not disclose an IOP. In the Final Office Action mailed February 2, 2005, the Examiner pointed to element 1844c of Fig. 21 in the Falik reference as disclosing the IOP. Page 6, lines 5-6. Appellants, however, respectfully assert that the Examiner's interpretation of element 1844c is incorrect. The Falik reference clearly states that element 1844c is an I/O *device* and not an I/O *processor*. *See* Col. 2, line 54. Further, there is nothing in the Falik reference that discloses or suggests that this I/O device 1844c is an I/O processor. In fact, the I/O device 1844 is only mentioned once in the Falik reference, and it is never described. *See* col. 2, line 54. It is merely acknowledged as being present. *Id.* Thus, it is clear that neither the Li reference nor the Falik reference, alone or in combination, discloses an IOP as recited in claims 1, 9, 16, and 24. For at least these reasons, Appellants respectfully request that the Board overturn the

[1] In the Final Office Action mailed on February 7, 2005, the Examiner stated that "the wording in the examiner's rejection (i.e., 'one with ordinary skill in the art would knowthat [the device] would contain these two features') is a statement of Official Notice." Appellants do not understand how this statement by the Examiner can be considered to be a use of Official Notice.

Examiner's rejections and allow independent claims 1, 9, 16, and 24 and the claims that depend therefrom.

5. **The Examiner's rejections of independent claims 1, 9, 16, and 25 are improper because the cited references fail to disclose either an embedded JTAG master that is controllable by the IOP or operative communication between the IOP and the JTAG master**

In addition to the reasons outlined above, Appellants also respectfully assert that the Examiner has not established a *prima facie* case of obviousness with regard to independent claims 1, 9, 16, and 24, because neither the Li reference nor the Falik reference discloses or suggests "an embedded JTAG master that is controllable by the IOP," as recited in claims 1, 9, and 24, or an "IOP and a JTAG master disposed thereon for operative communication with each other," as recited in claim 16. In particular, as described above, the Li reference does not disclose or suggest an IOP and, as such, certainly cannot disclose the above-recited claim features. Moreover, even if the Board were to accept the Examiner's "suggested" IOP, the Li reference certainly cannot be interpreted to disclose functionality for an admittedly undisclosed element.

The Falik reference cannot cure this deficiency in the Li reference, because (as described in greater detail above), the Falik reference merely includes a casual reference to an I/O *device* and not an I/O processor. Furthermore, even if the I/O device 1844c was considered to be an I/O processor, the Falik reference provides no indication that the I/O device 1844c even interacts with the debugger 1841 (cited by the Examiner as a JTAG master), much less controls it. *See* Falik, col. 2, lines 5-58 and Office Action mailed July 13, 2004, page 5, lines 21-22. As such, even if the Falik reference did disclose an IOP instead of an I/O device, that IOP could not be part of "an embedded JTAG master that is

controllable by the IOP," as recited in claims 1, 9, and 24, or an "IOP and a JTAG master disposed thereon for operative communication with each other," as recited in claim 16. For these additional reasons, Appellants respectfully request that the Board overturn the Examiner's rejections and allow independent claims 1, 9, 16, and 24 and the claims that depend therefrom.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

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8. **APPENDIX OF CLAIMS ON APPEAL**

1. A remote server management controller disposed in a managed server, the remote server management controller comprising:

an IOP;

an embedded JTAG master that is controllable by the IOP, the embedded JTAG master having a JTAG interface; and

at least one integrated circuit disposed in the managed server and connected for operative communication to the JTAG interface, and

wherein the JTAG master is configured to be accessed remotely through the remote server management controller to provide communication between a remote computer and the at least one integrated circuit via the JTAG interface.

2. The remote server management controller of claim 1 wherein the JTAG interface comprises an ITP interface that uses an ITP testing methodology.

3. The remote server management controller of claim 1 wherein the JTAG interface comprises an ICE interface that uses an ICE testing methodology.

4. The remote server management controller of claim 1 wherein the at least one integrated circuit comprises a microprocessor.

5. The remote server management controller of claim 1 wherein the at least one integrated circuit comprises a component of a chipset.

6. The remote server management controller of claim 1 wherein the JTAG master is configured to program the at least one integrated circuit.

7. The remote server management controller of claim 1 wherein the IOP is configured to be programmed to control the JTAG master to perform an initial test of the at least one integrated circuit when the managed server is initially powered up.

8. The remote server management controller of claim 1 wherein the IOP is programmed with descriptive data about the at least one integrated circuit.

9. A managed server, comprising:

a motherboard having at least one integrated circuit disposed thereon;

a remote server management controller in operable communication with the managed server, the remote server management controller comprising:

an IOP; and

an embedded JTAG master that is controllable by the IOP, the embedded JTAG master having a JTAG interface, the at least one integrated circuit connected for operative communication to the JTAG interface,

wherein the JTAG master is configured to be accessed remotely through the remote server management controller to provide communication between a remote computer and the at least one integrated circuit via the JTAG interface.

10. The managed server of claim 9 wherein the JTAG interface comprises an ITP interface that uses an ITP testing methodology.

11. The managed server of claim 9 wherein the at least one integrated circuit comprises a microprocessor.

12. The managed server of claim 9 wherein the JTAG master is configured to program the at least one integrated circuit.

13. The managed server of claim 9 wherein the at least one integrated circuit comprises a component of a chipset.

14. The managed server of claim 9 wherein the IOP is configured to be programmed to control the JTAG master to perform an initial test of the at least one integrated circuit when the managed server is initially powered up.

15. (The managed server of claim 9 wherein the IOP is programmed with descriptive data about the at least one integrated circuit.

16. A method of communicating with an integrated circuit in a managed server, the managed server having a remote server management controller in operative communication therewith, the remote server management controller having an IOP and a JTAG master disposed thereon for operative communication with each other, the JTAG master having a JTAG interface connected for operative communication to the integrated circuit, the method comprising the acts of:

receiving data at the IOP of the remote server management controller;

transmitting the data from the IOP to the JTAG master; and

transmitting the data from the JTAG master to the integrated circuit via the JTAG interface.

17. The method of claim 16, further comprising the act of programming the IOP to control the JTAG master to perform a boundary scan of the integrated circuit when the managed server is turned on.

18. The method of claim 16 further comprising the act of programming the IOP with descriptive data about the integrated circuit.

19. The method of claim 16 further comprising the act of programming the integrated circuit.

20. The method of claim 16 wherein the recited acts are performed preformed in the recited order.

21. A method of using a computer comprising:

connecting a computer to a remote server management controller disposed in a managed server; and

communicating with an integrated circuit disposed in the managed server via a JTAG interface associated with the remote server management controller.

22. The method, as set forth in claim 21, wherein communicating with the integrated circuit is controlled by an IOP.

23. The method, as set forth in claim 21, wherein the integrated circuit comprises a microprocessor.

24. A method of manufacturing a computer comprising:

disposing a remote server management controller in a server, the remote server management controller comprising:

an IOP;

an embedded JTAG master that is controllable by the IOP, the embedded JTAG master having a JTAG interface; and

an integrated circuit disposed in the managed server and connected for operative communication to the JTAG interface, and

wherein the JTAG master is configured to be accessed remotely through the remote server management controller to provide communication between a client computer and the integrated circuit via the JTAG interface.

25. The method, as set forth in claim 24, wherein the integrated circuit is located on a motherboard.